What is claimed is:

(1) A single integrated circuit microcontroller comprising:

an erasable/programmable non-volatile memory unit;

a read protection flag stored within said microcontroller; and

a logic portion which is adapted to detect when a special mode is activated, to check said read protection flag upon detecting a special mode, and to allow external access to said non-volatile memory unit only if said special mode is activated and said read protection flag is cleared.

(2) The microcontroller of claim 1 wherein said non-volatile memory unit is adapted to store certain firmware, and wherein logic portion is further adapted to alter said certain firmware if said read protection flag is set and said special mode is activated, and to clear said read protection flag after said firmware is altered.

(3) The microcontroller of claim 2 wherein said logic portion is adapted to erase said certain firmware if said read protection flag is set and said special mode is activated, and to clear said read protection flag after said firmware is erased.

(4) The microcontroller of claim 2 wherein said logic portion is adapted to program over said certain firmware if said read protection flag is set and said special mode is activated, and to clear said read protection flag after said programming is complete.

(5) The microcontroller of claim 1 wherein said logic portion is further adapted to erase said non-volatile memory unit if said read protection flag is set and said special mode is activated, and to allow external access to said non-volatile memory unit after said non-volatile memory unit is erased.

(6) The microcontroller of claim 1 wherein said read protection flag is stored within said non-volatile memory unit.

(7) The microcontroller of claim 1 wherein said erasable/programmable non-volatile memory unit comprises a flash memory unit.

(8) The microcontroller of claim 1 further comprising:

at least one input/output pin, and wherein said logic portion comprises:

switching logic which is adapted to selectively connect and disconnect said at least one input/output pin to and from said non-volatile memory unit; and

control logic which is communicatively coupled to said switching logic and which is adapted to detect when said special mode is activated, to check said read protection flag upon detecting a special mode, and to erase said non-volatile memory unit and clear said read protection flag if said read protection flag is set and said special mode is activated, said control logic being further adapted to selectively communicate signals to said switching logic, effective to connect said at least one input/output pin to said non-volatile memory only if said special mode is activated and said read protection flag is cleared.

(9) The microcontroller of claim 8 further comprising a micro-control unit which is selectively connected to said input/output pins and to said non-volatile memory unit by use of said switching logic.

(10) The microcontroller of claim 1 further comprising a random access memory unit which is communicatively coupled to said micro-control unit.

(11) The microcontroller of claim 10 further comprising a read-only memory unit which is communicatively coupled to said micro-control unit.

(12) The microcontroller of claim 11 wherein said micro-control unit comprises a microprocessor.

(13) The microcontroller of claim 8 wherein said control logic is communicatively coupled to said at least one input/output pin and is adapted to detect a special mode upon sensing a predetermined sequence of signals communicated to said at least one input/output pin.

(14) A single integrated circuit microcontroller comprising:

an erasable/programmable non-volatile memory unit including a first portion adapted to store certain firmware;

a read protection flag stored within said non-volatile memory unit; and

a logic portion which is adapted to detect when a special mode is activated, to check said read protection flag upon detecting a special mode, and to allow external access to said first portion of said non-volatile memory unit only if said

special mode is activated and said read protection flag is cleared.

(15) The microcontroller of claim 14 wherein said memory unit further comprises a second portion and wherein said logic portion is adapted to allow external access to said second portion of said non-volatile memory unit during said special mode when said read protection flag is set and when said read protection flag is cleared.

(16) The microcontroller of claim 15 wherein said logic portion is further adapted to detect an external request to access said first portion of said memory unit when said special mode is activated, to erase said certain firmware in response to said external request if said read protection flag is set, and to allow external access to said first portion of said memory unit only after said certain firmware is erased.

(17) The microcontroller of claim 15 wherein said logic portion is adapted to detect a request to access said first portion of said memory unit when said special mode is activated, to program over said certain firmware in response to said request if said read protection flag is set, and to allow external access to

said first portion of said memory unit only after said programming is complete.

(18) A single integrated circuit microcontroller having self-erase read protection, comprising:

a flash memory unit containing a read protection flag;

a processing unit;

a plurality of input/output pins;

at least one switching circuit which is adapted to selectively connect and disconnect said plurality of input/output pins to and from said flash memory unit and said processing unit;

a special mode detection circuit which is communicatively coupled to said at least one switching circuit and said plurality of input/output pins, said special mode detection circuit being adapted to detect when a special mode is activated, and to selectively generate a first signal and a second signal when said special mode is activated, wherein said second signal is communicated to said at least one switching circuit, effective to connect said plurality of input/output pins to said flash memory unit only when said special mode is activated; and

a flash memory control circuit which is communicatively coupled to said special mode detection circuit, and which is

adapted to receive said first signal, to check said read protection flag upon receipt of said first signal, to erase said flash memory unit and clear said read protection flag if said read protection flag is set and said special mode is activated, and to communicate a third signal to said special mode detection circuit when said read protection flag is cleared and said special mode is activated;

wherein said third signal is effective to cause said special mode detection circuit to generate said second signal only after receipt of said third signal, thereby preventing said plurality of input/output pins from being connected to said flash memory unit unless said special mode is activated and said read protection flag is cleared.

(19) The microcontroller of claim 18 wherein said special mode detection circuit is adapted to detect a special mode by sensing a predetermined sequence of signals on said plurality of input/output pins.

(20) A method for providing read protection for a microcontroller including an embedded programmable non-volatile memory unit having a first portion that stores certain firmware, and a special mode in which said programmable non-volatile

memory unit is externally accessible, said method comprising the steps of:

storing a read protection flag in said microcontroller;

detecting when said special mode is activated;

checking said read protection flag when said special mode is activated; and

allowing external access to said first portion of said memory unit only if said read protection flag is cleared.

(21) The method of claim 20 further comprising the steps of:

detecting a request to access said first portion of said memory while said special mode is activated;

erasing said first portion of said memory unit upon detecting said request if said read protection flag is set;

clearing said read protection flag after said first portion of said memory unit is erased; and

allowing access to said first portion of said memory unit.

(22) The method of claim 20 further comprising the steps of:

detecting a request to access said first portion of said memory unit while said special mode is activated;

reprogramming said first portion of said memory unit upon detecting said request if said read protection flag is set;

clearing said read protection flag after said first portion of said memory unit is reprogrammed; and

allowing access to said first portion of said memory unit.

(23) The method of claim 20 wherein said step of allowing external access to said first portion of said memory unit comprises electrically connecting said memory unit to a plurality of input/output pins.

(24) The method of claim 23 wherein said step of electrically connecting said memory unit to a plurality of input/output pins is performed by use of at least one switching circuit.

(25) The method of claim 24 wherein said special mode is detected by sensing a predetermined sequence of signals on said plurality of input/output pins.

(26) The method of claim 20 wherein said memory unit further comprises a second portion, said method further comprising the steps of:

detecting a request to access said second portion of said memory unit while said special mode is activated; and

allowing access to said second portion of said memory unit in response to said request when said read protection flag is set and when said read protection flag is cleared.